Claims

What is claimed is:

1. A method of fabricating an electronic device comprising:

implanting a dopant into an area of a semiconducting substrate, the implanted area being located within a region isolated by a dielectric isolator;

depositing a film stack over the implanted and dielectric isolator areas, the film stack including a first dielectric layer and a first polysilicon layer;

etching a dielectric window through the first dielectric layer;

depositing a second dielectric layer into the dielectric window and over the film stack;

etching the second dielectric layer anisotropically to form a first spacer;

etching portions of the film stack lying between the implanted area and the first dielectric layer anisotropically thereby forming an epitaxial via;

filling the epitaxial via with epitaxial silicon, thereby forming an epitaxial channel;
forming a second polysilicon layer over the epitaxial channel;

depositing a third dielectric layer over the second polysilicon layer and surrounding areas;

etching the third dielectric layer anisotropically to form a second spacer;

etching the first polysilicon layer;
depositing a fourth dielectric layer over the second polysilicon layer and the first polysilicon layer;

etching the fourth dielectric layer to form a third spacer; and

etching any remaining layers surrounding the third spacer down to substantially a level of the implant area.

2. The method of claim 1 wherein the film stack is comprised of a pad oxide, a first polysilicon layer, a nitride layer, and an oxide mask.

3. The method of claim 1 wherein the spacer is comprised of oxide.

4. The method of claim 1 wherein the first, second, third, and fourth dielectric layers are comprised of oxide.

5. An electronic device comprising:

a semiconductor substrate having thereon at least one region laterally enclosed by a dielectric isolation region, the region being implanted with a dopant, a topmost surface of the dielectric isolation region and the implanted region being substantially coplanar with a principal surface of the substrate;

an epitaxial channel disposed on the topmost surface of the implanted region and electrically coupled to the implanted region, a periphery of the epitaxial channel having been defined by a first dielectric spacer; and

a polysilicon region peripherally disposed to and surrounding the epitaxial channel, the polysilicon region at least partially overlaying the implanted region and isolated from direct electrical coupling with the implanted region by a dielectric layer.

6. The electronic device of claim 5, wherein the epitaxial channel is electrically coupled to the peripheral polysilicon region when a voltage exceeding a threshold voltage is applied to the epitaxial channel.

7. The electronic device of claim 5, wherein the epitaxial channel is electrically isolated from the peripheral polysilicon region when a voltage less than a threshold voltage is applied to the epitaxial channel.

8. The electronic device of claim 5, wherein the polysilicon region is circumscribed by a second dielectric spacer.

9. The electronic device of claim 5, further comprising a polysilicon cap on the topmost surface of the epitaxial channel, the polysilicon cap being circumscribed by a third dielectric spacer.

10. The electronic device of claim 9, wherein the polysilicon cap is a gate contact for a transistor.

11. The electronic device of claim 5, wherein the polysilicon region is a drain contact of a transistor.

12. The electronic device of claim 5, wherein the implanted region is a source contact of a transistor.

13. A method of fabricating an electronic device comprising:

implanting a dopant into an area of a semiconducting substrate;

depositing a film stack over the implanted, the film stack including a first dielectric layer and a first polysilicon layer;

etching a dielectric window through the first dielectric layer;

forming a first spacer within the dielectric window;

etching portions of the film stack lying between the implanted area and the first dielectric layer anisotropically thereby forming an epitaxial via;

filling the epitaxial via with epitaxial silicon, thereby forming an epitaxial channel;

forming a second polysilicon layer over the epitaxial channel;

forming a second spacer circumscribing the second polysilicon layer;

etching the first polysilicon layer; and forming a third spacer circumscribing the first polysilicon layer.

14. The method of claim 13, further comprising isolating the implanted area by a dielectric isolator.

15. The method of claim 13, wherein the first oxide spacer is formed by depositing a second dielectric layer into the dielectric window and over the film stack and then etching the second dielectric layer anisotropically to form the first spacer.

16. The method of claim 13, wherein the second spacer is formed by depositing a third dielectric layer over the second polysilicon layer and surrounding areas and anisotropically etching the third dielectric layer.

17. The method of claim 13, wherein the third spacer is formed by depositing a fourth dielectric layer over the second polysilicon layer and the first polysilicon layer and anisotropically etching the fourth dielectric layer.

18. The method of claim 17, further comprising etching any remaining layers surrounding the third spacer down to substantially a level of the implant area.